

IN THE CLAIMS

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1. (Previously Presented) A method for pulse width modulation comprising the steps of:
providing a pulse width modulator having n bits of resolution and a nominal time period P_n ;
supplying an additional timer to generate K associated states and having a timer period P_T , wherein K is greater than 2;
associating a modulator output value with each one of said K states; and
establishing a pulse width modulation update interval of $K \cdot P_T$.
 2. (Original) The method of claim 1 wherein P_T is an integer multiple of P_n .
 3. (Original) The method of claim 1 wherein said pulse width modulator includes an overflow bit.
 4. (Original) The method of claim 1 wherein $P_T = P_n$.
 5. (Previously Presented) A method for improving the resolution of an n bit pulse width modulator having a nominal time period of P_n , the method comprising the steps of:
supplying an additional timer having K associated states, wherein K is greater than 2, and a timer period of P_T ;
associating a modulator output value with each one of said K states; and
outputting a pulse according to said modulator output value during each time period P_n occurring within said timer period P_T during each one of said K timer states, whereby the resolution of said n bit pulse width modulator substantially equals $n + \log_2(K)$.
 6. (Original) The method of claim 5 wherein P_T is an integer multiple of P_n .
 7. (Original) The method of claim 5 wherein said pulse width modulator includes an overflow bit.

8. (Original) The method of claim 5 wherein $P_T = P_n$.
9. (Original) The method of claim 5 where P_T is other than an integer multiple of P_n and $P_T \gg P_n$.
10. (Original) The method of claim 9 wherein said pulse width modulator includes an overflow bit.
11. (Previously Presented) A computer program product for pulse width modulation comprising:
- a computer readable storage medium having computer readable program code means embedded in said medium, said computer readable program code means having:
 - a first computer instruction means for associating K timer states, wherein K is greater than 2, with a timer having a period P_T ; and
 - a second computer instruction means for reading a commanded pulse width modulation duty cycle;
 - a third computer instruction means for assigning an n bit modulator output value with each one of said K states according to said duty cycle.
12. (Original) The computer program product of claim 11 wherein said third computer instruction means updates said n bit modulator output value assigned to each state at time intervals of $K \cdot P_T$.
13. (Withdrawn) A method for controlling the brightness of a display using pulse width modulation comprising the steps of:
- receiving a commanded brightness level;
 - using an n bit pulse width modulator to assert a plurality of pulses in accordance with an output of said n bit pulse modulator wherein said modulator has a period P_n ;

assigning a modulator output value to each one of K states of a K state timer wherein said timer has a period P_T ;

outputting said plurality of pulses according to said modulator output value during each P_n period occurring within timer period P_T ; and

supplying power to the display in accordance with said plurality of pulses.

Cy 14. (Previously Presented) An apparatus for pulse width modulation comprising:
an n bit pulse width modulator having a nominal modulator period P_n ;
a timer to generate K timer states, wherein K is greater than 2, and having a timer period P_T ;

a computing device for assigning a modulator output value to each of said K states; and
whereby said modulator outputs a plurality of pulses according to said modulator output value during each P_n period occurring within timer period P_T and whereby said pulse width modulator has a resolution of $n + \log_2 K$.

15. (Original) The apparatus of claim 14 wherein said timer is included within said computing device.

16. (Original) The apparatus of claims 14 where P_T is an integer multiple of P_n .

17. (Original) The apparatus of claim 14 wherein P_T is other than an integer multiple of P_n and $P_T \gg P_n$.

18. (Original) The apparatus of claim 14 wherein said modulator further comprises overflow bit.

19. (Previously Presented) An apparatus improving the resolution of an n bit pulse width modulator having a P_n period, the apparatus comprising:

a timer to generate K timer states, wherein K is greater than 2 and having a timer period P_T ;

a computing device for assigning a modulator output value to each of said K states; and
whereby said modulator outputs a plurality of pulses according to a modulator output value during each P_n period occurring within timer period P_T and whereby the pulse width modulator has a resolution of $n + \log_2 K$.

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20. (Withdrawn) An LED backlit display comprising:
an array of LEDs;
an n bit pulse width modulator having a period of P_n ;
a computing device for assigning a modulator output value to each of said K states;
whereby said modulator outputs a plurality of pulses according to said modulator output value during each P_n period occurring within timer period P_T and whereby said pulse width modulator has a resolution of $n + \log_2 K$; and
a driver for supplying power to said array in accordance with said modulator output.

21. (Previously Presented) A method for improving the resolution of a hardware based pulse width modulator, the method comprising:

generating a pulse width modulated signal during a first time interval having a first modulator output; and

generating multiple further pulse width modulated signals during multiple succeeding time intervals having selected modulator outputs; and

repeating the generation of such pulse width modulated signals during the first and succeeding time intervals to provide an overall duty cycle having a desired resolution higher than the resolution of the hardware based pulse width modulator.

22. (Previously Presented) A method for improving the resolution of a hardware based pulse width modulator, the method comprising:

specifying a desired duty cycle;

determining a timer state;
if the state needs to be set at 100% duty cycle, setting the duty cycle to 100%;
otherwise, setting pulse width modulation of the pulse width modulator to an appropriate value for this state;
turning off a 100% duty cycle bit; and
incrementing a state counter for a next state.

23. (Previously Presented) A system for improving the resolution of a hardware based pulse width modulator, the system comprising:

means for generating a pulse width modulated signal during a first time interval having a first modulator output; and

means for generating multiple further pulse width modulated signals during multiple succeeding time intervals having selected modulator outputs; and

means for repeating the generation of such pulse width modulated signals during the first and succeeding time intervals to provide an overall duty cycle having a desired resolution higher than the resolution of the hardware based pulse width modulator.
